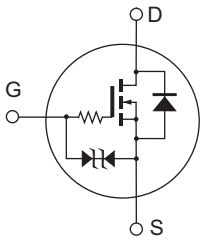
2SK2980

Features

- Low on-resistance
  $R_{DS(on)}$ = 0.2 Ω typ. (V_{GS} = 4 V, I_D = 500 mA)
- 2.5 V gate drive devices.
- Small package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is “ZZ–”

2SK2980

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	+12	V
		–10	V
Drain current	I_D	1.0	A
Drain peak current	$I_{D(pulse)}$ Note1	4	A
Channel dissipation	Pch Note2	0.8	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10μs, duty cycle ≤ 1 %

2. Value at when using alumina ceramic board (12.5 x 20 x 0.7 mm)

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 100 μA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	+12	—	—	V	I_G = +100 μA, V_{DS} = 0
		–10	—	—	V	I_G = –100 μA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1.0	μA	V_{DS} = 30 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±5.0	μA	V_{GS} = ±8 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 10 μA, V_{DS} = 5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.28	Ω	I_D = 500 mA, V_{GS} = 4 V Note3
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.5	Ω	I_D = 500 mA, V_{GS} = 2.5 V Note3
Forward transfer admittance	$\|y_{fs}\|$	1.2	2.0	—	S	I_D = 500 mA, V_{DS} = 10 V Note3
Input capacitance	Ciss	—	155	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	75	—	pF	
Reverse transfer capacitance	Crss	—	35	—	pF	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	V_{GS} = 4 V, I_D = 500 mA, R_L = 20 Ω
Rise time	t_r	—	30	—	ns	
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	30	—	ns	

Note: 3. Pulse test